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Università degli Studi di Napoli Federico II - Dipartimento di Fisica "Ettore Pancini"

Measurement and control electronic setup of superconducting quantum bits for the Quantum Computing Lab

General Specifications:

Compact microwave room-temperature electronics for the implementation of quantum algorithms on superconducting Quantum Processing Units (QPUs) composed by at least twenty (20) qubits.

It must include instruments and modules able to generate and measure microwave pulses in order to build quantum algorithms and diagnostic protocols on more than twenty superconducting qubits:

- **readout** modules for Quantum Non Demolitive (QND) measurements of the qubit state, i.e. able to generate and measure low-power microwave signals in a range from 2 GHz to > 12 GHz;
- **control/drive** modules for the excitation of superconducting qubits from 2 GHz to > 10 GHz, able to generate low-power signals in order to prevent leakage towards non-computational higher order energy levels in superconducting qubits;
- **frequency-tunability** modules, i.e. low-noise current/voltage arbitrary waveform generators, used to induce flux-tuning of the electrodynamics parameters of the QPU. Low-noise is a fundamental requirement for the reduction of dephasing and decoherence in the QPU. DC low-noise and ultra-stable current and/or voltage offset sources must be used to generate offset for flux pulsing. It is required that such signals are coupled via bias-tees with fast AWG (Arbitrary Waveform Generator) channels in the baseband regime > 250 MHz.

Pump generators for Josephson-based cryogenic Traveling Wave Parametric Amplifiers (TWPAs) are also requested, in order to amplify low-power response of the QPU at low-temperature (continuous wave signals with 2 GHz to > 12 GHz frequency range and maximum 5 dBm output signal for preventing saturation of the amplifiers).

Detailed Specifications:

Specifications on the main components of the setup: readout, control, tunability instruments and specifications for the acquisition/processing data.

Readout modules specifications (minimum 7 RF pulsed signal input/outputs).

- Operation frequency range from 2 GHz to > 12 GHz, in order to be compatible with cryogenic amplification electronics and cryogenic input and output readout signal lines in a dilution refrigerator for superconducting QPUs testing. The frequency resolution should be of ≤ 1Hz.
- Local oscillators and IQ-mixers should be integrated into the system for direct-RF pulse generation, without the need of further hardware.
- 1GS/s DAC-ADC rate, for fast high-performance readout pulsed schemes in superconducting qubits.
- Internal self-calibration tools for local oscillators leakage suppression and IQ-mixer corrections.
- Minimum readout pulse width of 4 ns with maximum 1.4 ns rise/fall time (10%-90%).
- Real-time shaping of arbitrary pulse shapes and their parameters is required with an update rate of maximum 4 ns. Pulse amplitudes, offset, modulation phase and gain must be FPGA programmable.
- Input channels must allow on-board processing of the measurement with typical averaging, integration functions and must allow thresholding.
- It must be possible to allocate arbitrary pulse-shapes and integration functions in order to minimize crosstalk and improve the readout fidelity of QPU.
- For output signals, spurious Free Dynamic Range (SFDR) > 50 dB is required in the range from 2 GHz to > 12 GHz.
- For output signals, phase noise should satisfy the following conditions:
    - < -100 dBc/Hz at 12 GHz and at 10 kHz offset;
    - < -140 dBc/Hz at 12 GHz and at 10 MHz offset;
    - < - 150 dBc/Hz at 3 GHz and at 10 MHz offset.
- Each single readout channel should allow for multiplexed readout of minimum 6 frequency tones in a bandwidth of > 700 MHz. Each frequency channel (resonator) in the multiplexed input must be processed individually by the FPGA for acquiring measurement results from each qubit. Each frequency channel must be scheduled individually and independently within the same module hence same input/output pair for the readout.
- Input channels should allow signals as low as -26 dBm in order to work in the single photon regime and must provide variable gain input stage with >25 dB of tunability.
- Readout probe tones should be generated by the FPGA, allowing full control of the amplitude, offset, modulation frequency and phase.
- SMA Input-output connectors.
- Readout memory for >100.000 I/Q values per qubit.

The following specifications are also required:

- Fully-integrated solutions where IQ-channels are internally integrated with up- and down-conversion stages for direct-RF output channels.
- Solutions where real-time operations are programmed fully-deterministic with the possibility of back-to-back playback of pulses without delay in between.

Control/drive modules specifications (minimum 20 RF pulsed signals outputs for drive of 20 qubits simultaneously):

- Operation frequency range from 2 GHz to > 10 GHz, compatible with typical superconducting qubit frequencies and different circuital designs. The frequency resolution should be of ≤ 1Hz.
- Control channels should allow output in the low-power regime -40 dBm to 5 dBm to prevent leakage towards higher-order non-computational levels in superconducting qubits.
- Local oscillators and IQ-mixers should be integrated into the system for direct-RF pulse generation, without the need of further hardware.
- 1GS/s DAC-ADC rate, for fast high-performance readout pulsed schemes in superconducting qubits.
- Internal self-calibration tools for local oscillators leakage suppression and IQ-mixer corrections.
- Minimum control/drive pulse width of 4 ns with maximum 1.4 ns rise/fall time (10%-90%).
- Control channels should allow multiplexed output of minimum 6 frequency tones in a bandwidth of 700 MHz, while each drive frequency channel can be controlled individually with real-time pulse parameters such as amplitude, offset, modulation frequency and phase.
- Real-time shaping of arbitrary pulse shapes and their parameters for implementation and correction of single- and multi-qubit gates, including virtual Z-gates, is required with an update rate of maximum 4 ns. Pulse amplitudes, offset, modulation phase and gain must be FPGA programmable.
- Pulses must be selectable from a local wave memory rather to avoid uploading from the host PC. The local wave memory should allow defining pulses with arbitrary shapes in a 1 ns time grid.
- Spurious Free Dynamic Range (SFDR) > 50 dB in the range from 2 GHz to > 10 GHz.
- For output control signals, phase noise should satisfy the following conditions:
    - < -100 dBc/Hz at 12 GHz and at 10 kHz offset;
    - < -140 dBc/Hz at 12 GHz and at 10 MHz offset;
    - < - 150 dBc/Hz at 3 GHz and at 10 MHz offset.
- SMA Input-output connectors.

The following specifications are also requested:

- Fully-integrated solutions where IQ-channels are internally integrated with up- and down-conversion stages for direct-RF output channels.
- Solutions where real-time operations are programmed fully-deterministic with the possibility of back-to-back playback of pulses without delay in between.

Pump modules specifications (minimum 8 RF signals outputs for pump generation):

- Operation frequency range from 2 GHz to > 12 GHz, in order to be compatible with TWPAs cryogenic amplification electronics. The frequency resolution should be of $\leq$ 1Hz.
- In order to prevent saturation of the TWPAs, pump output should be <-30 dB.
- Real-time shaping of arbitrary pulse shapes and their parameters is required with an update rate of maximum 4 ns. Pulse amplitudes, offset, modulation phase and gain must be FPGA programmable.
- Spurious Free Dynamic Range (SFDR) > 50 dB in the range from 2 GHz to > 10 GHz.
- For output control signals, phase noise should satisfy the following conditions:
    - < -100 dBc/Hz at 12 GHz and at 10 kHz offset;
    - < -140 dBc/Hz at 12 GHz and at 10 MHz offset;
    - < - 150 dBc/Hz at 3 GHz and at 10 MHz offset.
- SMA Input-output connectors.
- Each channel should have output switches that allow signal suppression < 60 dB.

The following specifications are also requested:

- Solutions where real-time operations are programmed fully-deterministic with the possibility of back-to-back playback of pulses without delay in between.
- The pump drives comply with the specifications of the control lines as depicted above, such that pump lines can be used as control lines when the following conditions hold:
    - the QPU device does not allow for multiplexed control over the analogue bandwidth requested in the control modules specifications;
    - the number of qubits of the QPU scale up to >20 qubits.

Flux-Tunability modules specifications (minimum 60 output DC current and/or voltage sources and minimum 50 pulsed voltage outputs):

- Output range for flux-offset current sources > ±50 mA, and > ± 4V for voltage sources, with 18 bit DAC resolution.
- Output range for pulsed flux signals > 4.5 V_{pp} in the frequency range from DC to > 250 MHz.
- Real-time shaping of arbitrary flux pulse shapes and their parameters is required with an update rate of maximum 4 ns. Pulse amplitudes, offset, modulation phase and gain must be FPGA programmable.
- Flux-pulses must be selectable from a local wave memory rather to avoid uploading from the host PC. The local wave memory should allow defining flux-pulses with arbitrary shapes in a 1 ns time grid.
- Minimum voltage flux-pulse width of 4ns with maximum 1.4 ns rise/fall time (10% - 90%).
- Step response with < 0.5 % overshoot. This should be shown explicitly via output plots.
- Noise for flux-offset should have the following requirements:
    - measured at +50 mA into 50 Ω with ± 50 mA range:
        - < 2.5 nA/√Hz @ 10 Hz;
        - < 0.8 nA/√Hz @ 1 kHz;
    - measured into high impedance with ± 4 V range:
        - < 70 nV/√Hz @ 2 Hz;
        - < 30 nV/√Hz @ 100 Hz.
- Voltage Noise density for flux-pulses at 1 Hz on a 50 Ω load should be < 1.5 $\mu V/Hz^{1/2}$.
- Offset stability of flux-voltage pulses generator should be <1.5 ppm/K with reference to full scale.
- Monitoring system of the generated offset currents through dedicated voltage monitors output must be available.
- Drift of the voltage source outputs for flux-offset should have the following requirements:
    - measured into high impedance with ± 4 V range: < 0.7 ppm/°C of range + 1.5 ppm/°C of output;
    - measured at + 50 mA into 50 Ω with ± 50 mA range: < 2.5 ppm/°C of full scale.
- Systems to avoid ground loops and interference prevention, e.g. no physical connections between the mains ground and the output channels, isolator boxes, *etc*…) are required for flux-offset. As an example, power supply may include gyrator filters to avoid ground-loop issues.
- Given the fact that flux-offset sources do not require fast synchronization with the host PC, USB connection is a possible alternative to Ethernet/LAN connection.
- Backup batteries should be provided together with flux-offset DC sources.

The following specifications are also requested:

- Higher voltage pulsed outputs for flux-tuning, in order to omit bias-tees coupling between DC sources and the AWG outputs.
- Specifications of AWG flux-pulses modules compatible on a certain extent with typical drive-pulses generators, in order to provide direct driving in case the number of qubits scales up.
- Dedicated isolation (galvanic, or similar) applied at mains power of the flux-offset and/or flux-pulses outputs to prevent ground loops and interference.

- DC sources directly powered from batteries, which are automatically charged via constant mains connection. It must be possible that batteries are charged within the same unit, without being disconnected from the system to avoid interruptions of the experiment.
- Solutions for flux-pulses generation where real-time operations are programmed fully-deterministic with the possibility of back-to-back playback of pulses without delay in between.

Acquisition/processing data specifications

- Internal/External instrument triggering:
    - The system should incorporate a 10 MHZ reference clock where all local oscillators, FPGAs and other clocks in the system are phase-locked.
    - Ability to input external clock sources as master clock at 10 MHz, or output the internal clock via SMA, USB or equivalent input-output connectors for synchronizing external devices.
    - Digital outputs, as many as analog outputs for triggering external devices, should accompany the control lines. The timing of generated pulses should be synchronized in standard ways with other laboratory equipment from other manufacturers. Trigger input should be incorporated to receive marker/trigger signals from external devices.
- FPGA supported parametrization of generated pulses should work in a fully-deterministic manner, with real-time generation of pulses and update of the pulse parameters for the control, readout and pump pulses, as described above. The FPGAs should incorporate sufficient memory to store local waves and instructions for typical experiments for qubit control and readout.

Programming for instrument interface:

- All drivers/API and interface layers should support Python programming language.
- Next to low level access, high-level programming should be possible for intuitive programming of pulse level and gate level definitions of pulses, and qubit operations by writing hardware diagnostic quantum circuits.
- Automated Calibration routines for typical quantum computing experiments, e.g. internal self-calibration tools for local oscillators leakage suppression and IQ-mixer corrections.
- Software tools for convenient coding, easy debugging, oscilloscope modes, visualization tools are required.

The following specifications are also requested:

- Drivers and parameters can be controlled by using QCoDes compatible open source drivers.
- Ability to program FPGA using VHDL (VHSIC - Very High Speed Integrated Circuit - Hardware Description Language), or alternative methods for low level access to FPGA without using VHDL.
- Ability to create wrappers around python API (Application Programming Interface), or around the low-level programming interface.
- Open-source software layers, both for high and low-level programming.

Programming for data acquisition, diagnostic procedures, calibration and analysis:

- One week free of charge training program: a week long training program should be provided to train the user and laboratory members for quick setup and start of the measurements in the first week of delivery. Tutorials, typical experimental notebooks and example code scripts should be provided for reference.
- A set of diagnostic protocols and tools to determine relevant parameters for Quantum Information Processing is required, like: single- and two-qubit gate-fidelity (Clifford-based randomized benchmarking and/or Quantum Process Tomography, *etc*...), operational crosstalk (Rabi cross driving, Multiplexed readout crosstalk, Residual ZZ, *etc*...), readout single-shot fidelity protocols.
- A set of control and read-out parameters optimization protocols (All-XY, Rabi, Ramsey, Motzoi calibration, Rabi flipping, etc.) for single-qubits and 2-qubits entanglement (calibration of latencies, pulse distortions corrections, Net-zero pulse tunability) is required.
- A set of diagnostic tools for quantum chip quality, like qubit coherence (relaxation, Ramsey and Spin-Echo interferometry, Carr-Purcell-Milbourne-Gill sequences), qubit frequencies and energy levels spectroscopy with two- or three-tone heterodyne spectroscopy, readout resonator frequencies and quality with heterodyne spectroscopy, coupling strength between elements e.g., resonator-qubit coupling and qubit-qubit coupling by using spectroscopy experiments, is required.
- Apart from low level programming, API layer and the set of diagnostic tools mentioned above, a complete high level software package that allows to utilize full functionality of the hardware is required. It must be possible to write any arbitrary program, to create arbitrary pulse sequences and readout schemes within the limits of the hardware. This high level software should be open-source to allow creating proprietary algorithms on top of the given functionalities.
- The high level software should support QCoDeS drivers to integrate with other existing experimental hardware and software frameworks.

The following specifications are also requested:

- Data analysis tools and curve fitting scripts for single- and two-qubit characterization.
- Software and/or programming scripts are open-source, and customizable by the user if necessary.

It must be guaranteed:

- Ethernet/LAN, and equivalent data connection, between the setup/instruments and a host pc, with data rate of at least 1GBit/s.
- A modular system where the ability to add input and output channels on demand is possible. It is preferred to have a system where the same hardware backplane, synchronization, feedback, software layers and other features are kept in case the system size grows.
- Synchronization of all channels for readout/control/tunability signals with a timing below 1 ns, with a jitter of few ps, without the need for further hardware equipment.

- The measurement outcomes must be distributed among the modules with low-latency feedback for the implementation of fast and reliable single- and multi-qubit gates, quantum error correction schemes, and for the distribution of at least 20 qubits channels with all-to-all connectivity in the same time window. Independent control of each sequencer and channel is required. The feedback operations should be performed among all the control and readout channels internally, without needing an external central unit, repeater or synchronization module.
- The system must be compatible with a well-documented and professionally maintained Python-based software stack to control the QPUs experiments, together with a high-level data acquisition platform compatible with Windows/Linux. Software to control the hardware that allow programming of all the functionalities and input and output channels as described in the sections below are required. The Customer shall have full accessibility to the source codes and have permissions to modify and develop the codes in the future.

It is requested the possibility to synchronize all the channels in the instruments/modules within the hardware (via backplane, internal links), without needing further cables in between separate hardware units. The system should be able to scale up to 100+ qubits with the same synchronization framework.

System Voltage: Power supply of 215-230 V/50 Hz. Maximum power consumption with full load of about 5 kW.

Rack: The system must be equipped with an Instrument rack, where all the products pursued will be placed.

Hardware service: free for the first three (3) years after delivery.

Technical Firmware/software support: lifetime free-of-charge.

- The seller should describe the technical support channels in the warranty period. The technical support channels should provide answers not longer than 48 hours after the questions are sent via email/phone/others, during the warranty period.
- Maintenance and product malfunction or product replacement during the warranty period should be described.

Lead time: six (6) months after order confirmation.